Investigations of Dose Rate Effects on CMOS Submicronic Technologies

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Abstract

Majority of the TOTAL DOSE evaluations of MOS devices are made by using Cobalt 60 sources at dose rates which are far from the real conditions found in the natural space environment. When geostationary satellites experienced dose rate around 1 to 2 Krad(Si) per year [1], the dose rate recommended by the two major test procedures vary from 30 Rad(Si)/hour up to 300Krad(Si)/hour. One can think that those test conditions do not reflect the permanent effects that could occur during the lifetime of the mission.

The objective of the study is to evaluate the dose rate effects on circuits representative of the TEMIC/MATRA MHS state–of–the–art CMOS technology used for space parts manufacturing and provide recommendations for future new CMOS technologies characterizations.

1. Introduction

Coupled with the reduction of governments’ budgetary, the space electronic components offering has been drastically modified. Hard commercial competitions request to optimize product selections. In that frame, the radiation tolerance of electronics is one of the key figures for cost aspect. In fact, over–estimation of the mission requirements, unnecessary margins impose the selection of rad–hard products when tolerant parts are neglected. On the other hand, the procedures used for radiation testing require dose rates which are verified far from natural conditions experienced by satellites. When geostationary satellites experienced dose rate around 1 to 2 Krad(Si) per year [1], the dose rates recommended by the two major test procedures [2][3] vary from 30 Rad(Si)/hour up to 300Krad(Si)/hour. One can think that those test conditions do not reflect the permanent effects that could occur during the lifetime of the mission.

The objective of the study is to evaluate the dose rate effects on circuits representative of the TEMIC CMOS technologies used for space parts manufacturing.

2. Technology

2.1. Technology hardening

The way how the degradations induced by ionization occur and growth in bulk CMOS technologies has been investigated since many years and is now pretty well understood. Two major critical paths have been determined as being responsible of degradations and considered as major concerns for radiation hardness. Ionization creates hole/electron pairs in oxide. Due to difference between velocity of electrons and holes, the last ones are trapped in the oxide and by the way, modify the threshold voltage of the devices.
For CMOS technologies, we have to consider 3 types of devices; NMOS, PMOS and parasitic N type structures. Previous characterization of active NMOS and PMOS transistors performed with CO\textsuperscript{60} gives a linear drift of the threshold voltage of 1mV/Krad(Si) at 100 Rad(Si)/hour up to 100Krad(Si). This drift is acceptable and no further work is conducted to harden the thin oxide. On the other hand, for complex functions, the first parametric derate occurs after exposure to few Krad(Si) and is mainly due to thick oxide (6000Å oxide) used for isolation of active regions: the reduction of the threshold voltage of N parasitic structure tends to create leaking path between VDD and GND and between Source and Drain of the N transistor (Bird’s beak effect).

The fig.2 gives the evolution of the power stand–by current of the memory irradiated at 2Krad(Si)/hour. The solution retained to harden this critical path is to increase the initial threshold voltage by adapting the dose of implant located under the thick oxide. As the drift of the parameter is linear with dose, the offset in the threshold voltage gives sufficient margin to withstand the dose requirements of all major space applications.

### 2.2. Choice of Test Vehicles

Two representative test vehicles have been selected for the purpose of the evaluation. One very low power 32Kx8BIT SRAM (HM65656E), Very Large Scale Integrated circuit offering 25000 transistors per mm\textsuperscript{2} and often used for large memory banks in space applications, and the Standard Evaluation Circuit (SEC) of the 1µ GATE ARRAY family developed on a 29K gates matrix (1500 transistors/mm\textsuperscript{2}). This paper describes only results gathered on the SRAM, the gate arrays showing not sufficient sensitivity at the total dose experienced.

These two test vehicles are manufactured with the Radiation Tolerant 0.85µm CMOS technology so–called SCMOS1/2 RT. This process has shown radiation tolerance in the order of 35Krad(Si) where, at a dose rate of few Krad(Si)/hour, the memory static power consumption begins to drift significantly. The tolerance is higher [50–80Krad(Si)] for GATE ARRAY because of the lower integration of the matrices.
3. Irradiation Plan

The irradiation plan has been established taking into account technical requirements:
- The maximum exposure time is limited to 1 year.
- Test procedure shall be representative of existing norms (ESA/SCC, MIL STD).
- 5 Samples are irradiated at each dose rate.
- Common intermediate doses are mandatory between the different dose rates used for easier correlations.

The maximum total dose deposited is limited to 40Krad(Si) correlated to the 15 years satellites missions. The dose rates choiced for the purpose of the evaluation are listed in table 1.

4. Electrical Measurements

Previous irradiations performed on this technology has demonstrated that most important degradations are induced by charge trapping and, at higher total dose, by reduction of the mobility.

<table>
<thead>
<tr>
<th>Dose rate (Rad(Si)/h)</th>
<th>Test Duration</th>
<th>Total dose [Rad(Si)]</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>365 days</td>
<td>8600</td>
</tr>
<tr>
<td>5</td>
<td>365 days</td>
<td>40000</td>
</tr>
<tr>
<td>10</td>
<td>180 days</td>
<td>40000</td>
</tr>
<tr>
<td>100</td>
<td>400 hours</td>
<td>40000</td>
</tr>
<tr>
<td>1800</td>
<td>22 hours</td>
<td>40000</td>
</tr>
<tr>
<td>1000</td>
<td>4 hours</td>
<td>40000</td>
</tr>
<tr>
<td>250000</td>
<td>11 min</td>
<td>40000</td>
</tr>
</tbody>
</table>

As the charge trapping is often affected by dose rate [4][5][6], and even if the totality of the parameters scheduled in the detail specification are all tested, we have focused our study on the following parameters:
- Static Power Consumption (ICCSB)
- Input Voltage compatibility (VIL/VIH)
- Output drivability (VOL/VOH)
- Dynamic parameters (Access Time)

The functionality is controlled after each step of irradiation and during annealing.

5. Test Conditions

The bias diagram used during the irradiation of the components is illustrated by the fig.3. The overall test set–up is:
- Power supply at 5.00V
- Static Bias during irradiation
- Annealing according ESA/SCC test method
- Table 7 of the ESA/SCC 9301/030 detail specification.
- Alternative test method for higher dose rate test (cf § 5).

The test methods of the norms require to test the parts within one hour after the end of the exposure. If applicable for most of devices, this requirement is often not realistic for complex products for which test programs are developed on specific VLSI testers (large pin count, high speed, large memory, ...). Irradiation facilities are often far from test facilities. So, to avoid long time annealing due to transport, we have developed a procedure to record parameters easy to test (Input/Output voltage, Stand–by current, Access or delay times, ...) in order to monitor the annealing of the parameters after irradiation. This is particularly the case for higher dose rates experienced (10K and 250Krad(Si)/hour)
6. Results and discussions

The table 2 gives the major sensitive parameters versus the dose rates at the dose of 40Krad(Si).

**Table2: Memory parameters at 40Krad(Si)**

<table>
<thead>
<tr>
<th>Dose Rate [Rad(Si)/h]</th>
<th>5</th>
<th>10</th>
<th>100</th>
<th>1800</th>
<th>10000</th>
<th>250 000</th>
</tr>
</thead>
<tbody>
<tr>
<td>ICCDR (µA)</td>
<td>427</td>
<td>537</td>
<td>385</td>
<td>3 200</td>
<td>91 000</td>
<td>84 000</td>
</tr>
<tr>
<td>ICCOP (%)</td>
<td>0,65</td>
<td>2,1</td>
<td>2,8</td>
<td>10</td>
<td>25</td>
<td></td>
</tr>
<tr>
<td>ICCSB1 (µA)</td>
<td>372</td>
<td>1 280</td>
<td>1 430</td>
<td>8 000</td>
<td>7 940</td>
<td>450</td>
</tr>
<tr>
<td>ICCSB1 (µA) WORST CASE</td>
<td>1400</td>
<td>1 800</td>
<td></td>
<td>382 000</td>
<td>388 000</td>
<td></td>
</tr>
<tr>
<td>VOL (V)</td>
<td>0,32</td>
<td>0,34</td>
<td>0,34</td>
<td>0,26</td>
<td>0,29</td>
<td>0,23</td>
</tr>
<tr>
<td>VOH (V)</td>
<td>4,5</td>
<td>45</td>
<td>4,5</td>
<td>4,5</td>
<td>3,96</td>
<td>3,97</td>
</tr>
<tr>
<td>VIL (V)</td>
<td>1,13</td>
<td>0,98</td>
<td>0,98</td>
<td>0,79</td>
<td>0,76</td>
<td>1,09</td>
</tr>
<tr>
<td>VIH (V)</td>
<td>1,67</td>
<td>1,83</td>
<td>1,82</td>
<td>1,91</td>
<td>1,87</td>
<td>1,81</td>
</tr>
<tr>
<td>TAVQV (µS)</td>
<td>44</td>
<td>53</td>
<td>45</td>
<td>49</td>
<td>64</td>
<td>49</td>
</tr>
</tbody>
</table>
Starting from the data of the table 2, one can observe that a dose rate effect is present. It affects mainly the power supply current which is relevant to the parasitic currents leading from charge trapping.

The following figures illustrate the evolution of some parameters versus dose and for various dose rates experienced during the study. A lot of data has been gathered during this study, but only the most interesting ones are described in this paper.

Figure 4 depicts the evolution of the Address access time versus dose. Globally, no significant drift can pointed out from the data.

**Figure 4. Dynamic versus dose for various dose rates**

![Figure 4](image)

Figure 5 gives the evolution of the operating current at 5 MHz. This parameter stay stable over the dose range tested, so no derating in power calculation is necessary.

**Figure 5. Operating current versus dose for various dose rates**

![Figure 5](image)
Figure 6 confirms that thin oxide used for transistor gates have sufficient intrinsic hardness and is not affected in the dose range tested.

**Figure 6.** Input low voltage versus dose for various dose rates

The figures 7 and 8 have to be read together. In fact, they depicting the same phenomenon which is the reduction of the transconductance of the N transistor used in the output buffer. The curves show significant degradations starting 35Krad(Si) which recover after high temperature annealing.

**Figure 7.** Output low voltage versus dose for various dose rates
Other interesting parameter which degrades significantly is the ICCSB1 WORST CASE which reflects the current passing through the device when all the N transistors which were irradiated ON (+5V on the gate) are measured OFF (0V on the gate). In this case, the leakage is maximum because not limited by the P transistor of the inverter. In order to have a better understanding of what is the evolution of this current versus dose rates, additional results gathered during Radiation Lot Acceptance Testing (RLAT) or evaluation testing are analyzed. The figure 9 illustrates the increasing leakage current of one memory cell irradiated up to 40Krad(Si) versus dose rate.

The irradiations at dose rates lower than 5–10 Rad(Si) per hour induce lower degradations. A significant improvement in the behavior of the leaking currents can be observed for dose rates below 10 Rad(Si)/hour. The experiment conducted at 1 Rad(Si)/hour is still going on, the 40Krad(Si) level being reached during 1998.

These results show the interest of experiencing very low dose rates when introducing new technologies to market. Space introduction lead times seem to be in accordance with majority of space applications requirements to authorize experiments at dose rates in the range of 5 to 10 rad(Si)/hour. This could be rearranged when scientists will establish recognized procedures.
7. Further works

The removal of the charges trapped in the oxide during high dose rate exposure can be achieved through high temperature baking. This is a requirement of both the MIL STD and the ESA/SCC test methods. By using irradiation continued by various temperature/time duration annealing and with demonstration of the applicability of the theory of linear systems, the extrapolation of behavior at various dose rate including space range ones shall be possible.

8. Conclusions

The dose rate effects on TEMIC 0.85μm CMOS products manufactured using radiation tolerant technology have been successfully assessed during irradiation campaigns held during 94. Different dose rates experienced have shown a significant improvement of the tolerance for dose rates lower than 10 rad(Si)/hour.

The dose rates imposed by the norms exceed the degradations that are induced by natural outer space radiation environment.

Acknowledgments

We thank J.P. DAVID and many other members of the DERTS department for their technical assistance. Special thanks is also given to T. CARRIERE of Matra Marconi Space.

9. References