High Speed 15 ns 4 Mbits SRAM for Space Application

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Abstract

A high speed 15 ns 4 Mbits asynchronous SRAM, 500 Astand-by current, 300 Krads total dose tolerant, has been developed for space applications, using a hardened 0.25 micron 4 layers metal full CMOS process. A hierarchical organisation per IO bits has been used to achieve high speed as well as low dynamic consumption, also suited for simple SEU (single event upset) induced error corrections, allowing mitigation with classical EDAC corrector. The product operates within 3 to 3.6V, and ambient temperature from -55 to +125°C. A high density die size of 68.3 mm² allows the use of a specific 36-pins dual in line flat pack package with a 500 mils width, making this product very competitive against SEU hardened chips. Successful silicon results are presented as well as radiation tests up to 300 Krads.

1. Architecture

Due to the by 8 format (i.e. 512k x 8), the memory is divided in 8 areas of 512K x 1 bit and 1 control area. The floorplan of the architecture is illustrated in Fig. 1(a) Each area of 512K x 1 bit contains 4 plans. As shown in Fig. 1(b) each plan of 128 Kbits is divided in 4 memory arrays to reduce the bit line length and thus the parasitic capacitance to improve the access time. Each basic array contains 256 rows and 128 columns, ie. 32 Kbits. The columns and block decoders - as well as write and read amplifiers - are placed between the up or down memory arrays. For each plan of 4 arrays the row decoder is common and placed in central position between the 2 right and the 2 left memory arrays. This hierarchical address decoding allows low operating consumption without losing access time.

The main control area, as shown in Fig. 1(a), contains the address pre-decoding, the ETD clock circuitry (Edge Transition Detection), the control part and the internal voltage regulator. The TTL input buffer and the data output buffer are directly placed near their bonding pad.

2. Regulator

The SRAM 4 Mbit uses an internal voltage regulator, because the standard low voltage devices of the 0.25 m process sustain 2.5 ± 0.3V only. High voltage devices with thicker oxide devices are used for 3.3V TTL interface.

The regulator provides an output voltage of 2.5V with an input supply voltage ranging from 3 to 3.6V. Its output voltage supplies all the memory blocks except the output buffers. The maximum supply DC current is 150 mA.

The structure of this regulator is based on a bandgap. An amplifier is used as a follower and it has a reference input voltage at 1.2V (bandgap), and the value of the output voltage is set by a bridge of resistors. A capacitor of 1 nF improves the stability of the amplifier and makes it possible for the regulator to maintain the output voltage to 2.5V when there is a maximum peak current of 500 mA.
3. Dynamic Circuit

To achieve a fast access time a dynamic operating mode is implemented. For each input excepted data, i.e. address and control inputs, each signal transition is detected thanks to an Edge Transition Detection (ETD) circuit. The ETD circuits enable the generation of internal clocks: pre-charge, read or write pulses and latch controls. During the read operation an output buffer latch is used to reduce the operating consumption at low frequency. Fig. 2(b) illustrates the timing waveform of the schematic read diagram shown in Fig. 2(a). To adjust the pre-charge time without increasing the noise, all the columns not selected are held in pre-charge. The chip select input is also used as the general input gating of all input buffers, data input included, to achieve full stand-by mode.

4. Read Datapath

To reduce access time and improve the noise immunity of the chip, a full differential datapath from the memory cell to the output buffer is used, as shown in Fig. 2(a). This differential scheme [1,2] allows to balance the pair of complementary lines along the read datapath at the beginning of the reading phase thanks to a short balancing pulse; this results in a faster and reduced double voltage swing of these data buses which is transmitted to the amplifier stage. A pre-amplifier with a voltage gain of 2 is
placed near the pass gate that connects the bit lines. It translates the VDD referenced voltage of the bit lines to a VDD/2 differential signal. The pre-amplifier block is followed by a 2nd stage full differential amplifier. It amplifies the input data and drives 2 differential NMOS transistors with open drain connected to the data bus. The data bus is connected near the output pad to cross-coupled transistors PMOS and a PMOS pull-up. When the read signal is not selected, the differential data bus is loaded and balanced to VCC by 2 pull-up PMOS. During a read access the pull up PMOS are disabled: the cross-coupled transistors (PMOS) only load the bus which is driven by the NMOS transistor of the sensamp. A last stage made with a differential amplifier supplies the data at the output buffer. The first stage of the output buffer converts the internal data signal (2.5V) to a TTL level signal (3.3V) and stores it in a latch. The second stage, made with high voltage transistors supplies TTL level at the outputs.

5. Fabrication

The 6 transistor's memory cell views, layout and silicon, are illustrated in Fig. 3a and Fig. 3b. The final chip is illustrated in Fig. 4.

Fig. 3a Memory Cell Layout

Fig. 3b Microscopic View of Memory Cell

From an 8-inch wafer fabrication the product has been processed using a specific hardened version of the 0.25 m 5 metal layers Atmel, thanks to an additional implant on NMOS device trench isolation. Compared to a not tolerant process, the cell performances (stability, read current, stand-by leakage) are adjusted taking into account the transistor threshold shift and width reduction due to hardening implants. Only 4 metal layers are used, the fifth metal layer doesn’t help density, especially in memory cells. Low voltage devices for the 2.5V logic core use 50A oxide thickness at 0.24 m minimum channel length, while high voltage devices for 3.3V compatibility for input/output buffers used 80A oxide thickness at 0.50 m minimum channel length.
6. Performance Results

The product has been prototyped in its package and electrically characterised for 3.3 ± 0.3V, with an ambient temperature from -55 to +125°C. The chip was 100% functional at first silicon.

The high density 500 mils 36 pins FP package is shown in Fig. 5.

![Fig. 5 Chip Package](image)

The read access time, as shown in Fig. 6, has been measured on a tester in worst case conditions, i.e. at 125°C at 3V: the measure before calibration gives 15.5 ns for the both rising edge and falling edge of the worst case access time by address change; taking into account that hardware tester conditions are worse than those defined in the specification, (i.e. input slope, output current and 80 pF capacitor output load), the final calibrated result leads to a read access time better than 12 ns under the 15 ns specification with a good margin.

![Fig. 6 Read Access Time Measurements](image)

The stand-by current has been measured around 300 A for a 500 A target specification, as well as the 2V data retention current is better than 200 A.

The operating current is at 150 mA in worst case conditions, remains to be improved in the final release.

The new ESD (Electro Static Discharge) structure used has been successfully validated into class 3 (>4001V).

Radiation tests using Cobalt 60 source in accordance with MIL 1019.5 test method, up to 300 Krads exhibit excellent latch-up immunity and total dose capability without any drift on leakage currents or performances after annealing, demonstrating the absence of rebound effect.

7. Conclusions

The development of these 4 Mbits asynchronous SRAM on a specific hardened process version of the 0.25 mAtmel process is successful. The product fully meets its initial military range specification, e.g. 15 ns access time, 500 A stand-by current, 100 Krads tolerance, making this product a high speed and high density (die and package) solution for space applications. The product is currently in qualification phase. The product and technology are ready for industrialisation, and sampling is currently being performed.
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9. References
