Abstract—Space applications have very stringent requirements in terms of system integration and packaging density efficiency. For instance, the on-board data processing package for Telecommunication Digital Payload requires large and fast memory resources. Despite the diminution of the Power Supply level, the power consumption of the application, as well as its size and weight has increased.

The system integration goals cannot be met by integrating new functions because of the niche nature of the space market which doesn't allow to amortize the cost of new designs with every new silicon technology generation, or the merging of antagonist technologies on the same die (CMOS and AsGa, Analog and Digital, ...). The packaging density, as it will be described, can be improved through specific 2-D package styles (BGA like) and specific die assembly technics (flip-chip), but, so far, it was not sufficient to offer an affordable answer to both challenges: system integration and packaging density.

A solution for miniaturizing these applications is the use of a 3-D interconnection technology allowing significant board space and weight reduction as well as performance enhancement by reduction of the interconnection parasitic elements and buffer stages. In addition, this is a competitive alternative to monolithic larger size memories, potentially minimizing or delaying next generation development costs. The paper will describe the technology and the performances of a cost effective, very integrated and versatile 16 Mb to 64 Mb SRAM Module designed within a consortium including ATMEL, France, and 3D PLUS, France. This Memory module achieves a density of 5 to 20 Mb SRAM per cm² and 0.11 to 0.45 g per 1 Mb SRAM. It is based on monolithic 1 Mb or 4 Mb RAD Tolerant SRAM die from ATMEL and is integrated using the 3D PLUS space qualified 3-D packaging technology. The 3-D technology being ideally suited to System-In-Package applications (e.g. computer modules, ...) was already base lined for various European Space Missions like Rosetta, Mars Express,…and the paper will demonstrate how it helps populating an innovative product and packaging road map for Space applications.

INTRODUCTION

The pace at which new IC semiconductor technologies are introduced (Moore’s law resulting in the introduction of a new technology twice denser than the former every 18 months) is so high that it is incompatible with the pace of the Space Industry. Indeed, this niche market’s nature doesn’t allow the design of new ASIC libraries, memories or processors with every new technology.

Until now, the hybrid or MCM solutions answered this problem by accommodating more functionality into the same size/volume by putting together ‘die’ on a 2-D substrate instead of ‘packaged die’ on a board. These solutions, however, had the following limitations:

- the resulting interconnection density between dies necessitates very thin and expensive substrate manufacturing processes (less than 25 µm via diameter and line width) in order to keep the ‘package area’ savings after layout of the circuit,
- the size of the 2-D substrates is limited by the mechanical environments (vibration, shocks, thermal cycles) it has to survive and by its ceramic or metal package size and weight at board level trade-off,
- the MCM test complexity and cost increased drastically due to highly embedded components and to the availability/non availability of Known Good Dice.

Today, beyond the availability of denser space qualifiable semiconductor technologies, the race for more integration results into two types of packaging developments related activities:

- Denser individual screened packages which can be achieved through BGA type of solutions and flip-chip
die assembly processes in conjunction with well known and qualified surface mounting technologies,

- New type of MCMs, allowing for denser integration while maintaining, if not improving the reliability of the resulting product. One of the most promising example is the 3D PLUS technology, which allows to vertically stack dice of heterogeneous sizes and semiconductor technology. This 3-D technology allows a full die up screening prior to putting them together and uses well known assembly sub-technologies, which makes the technical solution very price and lead-time competitive.

This paper reviews the various individual packaging approaches proposed by ATMEL and describes the technology and the performances of a cost effective, very integrated and versatile 16 Mb to 64 Mb RAD Tolerant SRAM 3-D Module designed for Space application within a consortium including ATMEL, France, and 3D PLUS, France.

3-D technology System-In-Package applications (e.g. computer modules, …) were already base lined for various European Space Missions like Rosetta, Mars Express, Envisat… and the paper will demonstrate how it helps populating an innovative product and packaging road map for Space applications.

ATMEL’S APPROACH FOR INDIVIDUAL PACKAGING SIZE REDUCTION : BGA AND FLIP-CHIP

The main limiting factor for the package size reduction results from the exploding I/O count of the current dice.

Indeed, high density interconnection solutions have to be found at package I/O and die assembly and interconnection levels.

Package Mounting Technology Approach :

For the most complex type of ICs used in space applications, i.e. ASICs, the race for more gates per chip (current latest announcements report up to 7-10 M used gates) directs always to offer higher pin count packages. Therefore, the traditional way of packaging them into quad flat packages is no longer competitive for size and weight.

For instance, a 352 pins JEDEC package has a ceramic body which is 48x48 mm when the packaged die is only 15x15 mm max (i.e. 90% of resulting area loss), and its weight is close to 30 g.

The consensus in the Semiconductor Industry is to go for a type of BGA. But for space applications, many BGA solutions are not suitable due to the harsh climatic and mechanical environments. In the most harsh environment applications, the consensus is to go for a column grid type of BGA. ATMEL made the choice of the NTK SCI CLGA technology more than 5 years ago, due to the fact that it was the one which offered the greatest potential for achieving or getting the closest to the space requirements.

![Photo n° 1 : NTK SCI CLGA Package chosen by ATMEL](image)

The available packages (cf. photo 1) are as shown in the following table:

<table>
<thead>
<tr>
<th></th>
<th>Signal pins</th>
<th>Core power pins</th>
<th>Package body size (mm x mm)</th>
<th>Column pitch (mm)</th>
<th>Column array size (mm x mm)</th>
<th>Availability</th>
</tr>
</thead>
<tbody>
<tr>
<td>CLGA349</td>
<td>333</td>
<td>16</td>
<td>25x25</td>
<td>1,27</td>
<td>22,86</td>
<td>Y</td>
</tr>
<tr>
<td>CLGA472</td>
<td>440</td>
<td>32</td>
<td>29x29</td>
<td>1,27</td>
<td>26,67</td>
<td>Y</td>
</tr>
<tr>
<td>CLGA576</td>
<td>532</td>
<td>44</td>
<td>29x29</td>
<td>1</td>
<td>23x23</td>
<td>1H03</td>
</tr>
<tr>
<td>CLGA625</td>
<td>581</td>
<td>44</td>
<td>29x29</td>
<td>1</td>
<td>24x24</td>
<td>2H03</td>
</tr>
</tbody>
</table>

Therefore, CLGA versus QFP package, saves huge board area, but also weight as a CLGA 349 is only 10 g.

Die Assembly and interconnection Approach :

The next limiting factor for further reducing the package size is the die assembly process which is still the traditional wire bonding one: for a die of 13x13 mm, we need a cavity size which is almost 28x28 mm, including the lid package seal ring. The cavity size over head is twice the die size for large ones, but when one go to smaller die, the over head can grow to almost 4.

Moreover, the self parasitic effect generated by the wire bond severely limits the package’s electrical bandwidth and generates power supply level oscillations and ground bounce problems.
ATMEL has started the development of a flip chip technology qualifiable for space use: it is implemented in 2 steps:

- First, to evaluate the reliability of the die package interface using flip chip, a test vehicle is currently on going using our TSC695F Sparc processor, assembled onto a 195 pins CSP, with 1 mm ball pitch. The resulting package, presented in photo n° 2, is 15x15 mm for a die which is 11x11 mm, resulting in a size overhead smaller than 1,4.

- The second will be to extend the obtained technology to an hermetically qualifiable solution: we expect from such an approach to achieve a package size overhead, versus the die size, close to 1,3 for our largest die (15x15 mm) and, anyway, below 2 for our smallest ones (6x6 mm).

The expected benefit will be the ability to drastically reduce the CLGA land pitch to a point where, even for the most complex package currently under consideration (625), the land array size will be below 20x20 mm. A 0.8 mm pitch will then result in a land matrix size of 19,2x19,2 mm. This will no longer require the use of an SCI, and balls will make it, resulting in additional weight saving.

Photo n° 2 : TSC695F Sparc processor assembled onto a 195 pins CSP with the flip-chip technology.

Figure 1 : The 3-D interconnection Concept by 3D PLUS

3-D Technology Concept :

3D PLUS technique of interconnections in 3 dimensions of all types of components (Active, Passive, Magnetic, Optoelectronics and MEMS) is presented in figure 1.
3-D Technology Process Description (Figure n° 2) :

The original 3-D technology is based on the stacking of electronic components (chips, plastic or ceramic packages, TSOP, QFP, CSP packages, sensors) placed on a film identical to the one used by smart card manufacturers.

These films can be individually tested and submitted to burn-in to obtain high reliability flex or Known Good Flex prior to the 3-D stacking operation.

After the stacking of components and molding of epoxy resin to make the cube, a sawing is made in order to reveal the sections of the conductors on each level.

The sides of the cube are plated by depositing nickel and gold metallic layers, through techniques largely used in the printed circuits field.

The interconnection of the components is carried out by laser direct patterning.

The 3-D Module is then submitted to the relevant screening and test sequence for Space Applications.

3-D Technology Features and Benefits :

The components are stacked up: this technology allow gaining a factor of at least 10 on weight and volume of the components comparing to existing solutions. Its implantation area is always ‘2*N’ time better than the equivalent 2-D solution, N being the number of layers in the 3-D Module.

The interconnection is reduced and simplified. Electronic performance is significantly improved as parasitic effects (resistance, inductance and capacity) are reduced in approximately the same proportions as the reduction in volume.

The components are fixed into resin. The application’s resistance to harsh environments (vibrations, shocks, thermal cycles, humidity,…) is enhanced by the intrinsic characteristics of 3DPLUS technology.

3DPLUS patented Manufacturing processes use simple and well known technologies, leading to flexibility and short development time of new designs; and cost effectiveness and short manufacturing lead times for the recurring models.

The components can be shielded to decrease electrical noise and parasitic effects; and to provide shielding against radiation (1 mm loaded epoxy equivalent to 1 mm of Aluminum).

The ‘Cold’ plating Process used for the 3-D interconnection ensures its compatibility with future lead free soldering processes where the soldering temperature will be around 25°C higher than today.

Figure n° 2 : The 3-D interconnection process by 3D PLUS
DEVELOPMENT OF A VERSATILE 16 MB TO 64 MB SRAM 3-D MEMORY MODULE

On-board data processing for Telecommunication Digital Payload requires large and fast memory resources. Despite the diminution of the Power Supply level, the power consumption of the application, as well as its size and weight, has increased.

The use of a 3-D interconnection technology will allow a significant board space and weight reduction, as well as a performance enhancement, through the reduction of the interconnection parasitic elements and buffer stages. In addition, it would be a competitive alternative to larger (next generation) monolithic memories. The design of a true 16 Mb SRAM would theoretically have required a 0.09 \textmu m technology!

Module Definition:

The 16 Mb Rad Tolerant SRAM Memory Module embeds 16 dice of ATMEL RAD Tolerant 65609E 1Mbit SRAM and their 16 decoupling capacitors, organized in 8 layers of 2 dice and capacitors each.

The memory module block diagram is presented in figure 3.

The module memory organization can be modified from 2 M * 8 bit to 1 M * 16 bit by re-routing the basic memory I/Os with a simple laser plot software modification.

Thus, the replacement of the basic 1 Mb memory by the 4 Mbit memory will lead to a 64 Mb Rad Tolerant SRAM Memory Module.

The addition or deletion of layers and the modification of the laser plot software will easily transform the 16 Mb Memory Module into a 8 Mb, 32 Mb, or 64 Mb Memory module.

Basic Layer layout:

The Basic memory layer is presented in photo 3 and 4. It evidences very short electrical interconnection between dice, the interconnection between the sixteen dice being then the height of the module, i.e. 16 mm max. This line length is about 10 times shorter than the equivalent line on a board.

Moreover, test points can be observed in the periphery of the flex. They are used to test the memory with the manufacturer program and can also be used for the memory burn-in powering if required by the screening sequence.

![Figure n° 3 : 16 Mb SRAM Memory Module Block diagram](image3.png)

![Photo n° 3 : 16 Mb Memory Module basic Layer](image4.png)

![Photo n° 4 : 1 Mb SRAM Memory and Decoupling Capacitor Zoom view](image5.png)
16 Mb Module design result:

The developed Memory Module mechanical drawing is presented in figure n° 4 and photo n° 5.

The resulting size and weight is second to none: 0,2 cm² and 0,45 g per Mbit respectively. The ATMEL newest SRAM, which is a monolithic 4Mbits, achieves respectively 0,8 cm² and 1 g per Mbit. The performance detail is presented in table 1.

The Memory Module is packaged into a 64 pins Flat Pack package (pitch 0,635 mm) well known by the Space industry equipment manufacturer and whose mounting is already qualified for most of them. Moreover, the memory module weight is also compatible with the pick and Place equipments.

Module availability and qualification for Space application:

The 16 Mb Memory Module is completed and the product is available from both 3D PLUS and ATMEL Standard Products catalogue in EM and FM quality grades.

3D PLUS Technology Process Identification Document and Manufacturing Line were successfully evaluated/qualified for Space Applications by NASA, ESA and CNES in 2001.

The relevant results and various information can be found on the NASA web site.
<table>
<thead>
<tr>
<th>Capacity</th>
<th>Memory Organization</th>
<th>Weight (g. per 1 Mb SRAM)</th>
<th>Density (Mb SRAM per cm²)</th>
<th>Area Savings (1)</th>
<th>Weight Savings (1)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Mb</td>
<td>Basic Package QFPL</td>
<td>2,18</td>
<td>0,45</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>4 Mb</td>
<td>Basic Package QFPL</td>
<td>0,8</td>
<td>1,36</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>16 Mb</td>
<td>16 * 1 Mb Die</td>
<td>0,45</td>
<td>5</td>
<td>93 %</td>
<td>78 %</td>
</tr>
<tr>
<td>64 Mb</td>
<td>16 * 4 Mb Die</td>
<td>0,11</td>
<td>20</td>
<td>95 %</td>
<td>85 %</td>
</tr>
</tbody>
</table>

(1): The savings are calculated against the equivalent function designed with 16 * 1 Mb or 4 Mb SMT single packages.

Table 1: 16 Mb and 64 Mb SRAM Packaging Performances Summary

CONCLUSION : EXTENSION TO OTHER SYSTEM IN PACKAGE PERFORMANCES, ROAD MAPS

ATMEL selected 3D PLUS technology as a complementary packaging solution for higher levels of integration. Both companies have started joint development activities whose first result is a 16 Mbit SRAM built by stacking 16 dice of ATMEL 65609E 1Mbit SRAM, organized in 8 layers of 2 die each.

The resulting size and weight is second to none: 0,2 cm² and 0,45 g per Mbit respectively. Our newest SRAM, which is a monolithic 4Mbits, achieves respectively 0,8 cm² and 1g per Mbit.

When we go for stacking 16 die, and later on 32, of the new 4Mbit SRAM, we will drastically improve both characteristics by a factor of 4 and 8 respectively.

ATMEL and 3D PLUS have also demonstrated their willingness and ability to undertake long term development in new packaging technologies which bring huge benefits to the space industry in term of integration (size and weight) and performances.

The possibility to package dice of various sizes opens the door to another step towards system integration by assembling together processors, memories and system logic as presented in photos 6 to 8.

As presented in its Products Road Map (figure n° 4), ATMEL is keen to consider this opportunity when a space customer is confident for going this way. The following ATMEL products and technology roadmap illustrates the fields where those new packaging technologies help populating it.

Photo n° 6: 3D PLUS 3DSP21020 Computer Module embedding the ATMEL TSC21020F Floating Point DSP + SRAM, SDRAM, FLASH and PROM Memories + co processors FPGAs + for Space Application

Photo n° 6 bis: X-Ray photo of the 3D PLUS 3DSP21020 Computer Module showing the 11 integrated layers
Photo n° 7: 3D PLUS EPIC Memory Modules (Electrical Power In Circuit): Memory module with integrated decoupling capacitors.

Photo n° 8: 3D PLUS Stacked CSP Memory Modules

Figure n° 4: ATMEL products and technology roadmap